What is Claimed is:

1. A method of forming a structure having a textured surface for a semiconductor assembly comprising:

forming hemi-spherical grain silicon over a supporting substrate; and

forming epitaxial silicon directly on the hemi-spherical grain silicon.

2. The method of claim 1, further comprising forming an amorphous silicon layer on the supporting substrate prior to the formation of the hemi-spherical grain silicon.

3. The method of claim 2, wherein the amorphous silicon layer is formed by decomposing SiH_4 at approximately 500°C.

4. The method of claim 2, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

5. The method of claim 1, wherein the hemi-spherical grain silicon is formed by decomposing DCS ($Si_2H_2Cl_2$) in an H_2 and HCl environment at about 550 to 1000°C.

6. The method of claim 1, wherein the epitaxial silicon thickness is approximately 100Angstroms.

7. The method of claim 1, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

8. The method of claim 7, wherein the number of cycles performed is 5 cycles.

9. The method of claim 1, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

10. A method of forming a memory cell for a semiconductor assembly comprising:

forming an access transistor to a storage capacitor;

forming a conductive plug connecting to a source/drain of the access transistor;

forming hemi-spherical grain silicon on the conductive plug; and

forming epitaxial silicon directly on the hemi-spherical grain silicon.

11. The method of claim 10, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

12. The method of claim 10, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

13. The method of claim 10, wherein the epitaxial silicon thickness is approximately 100Angstroms.

14. The method of claim 10, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

15. The method of claim 14, wherein the number of cycles performed is 5 cycles.

16. The method of claim 10, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

17. A method of forming a storage node capacitor plate for a semiconductor assembly comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material; and

forming epitaxial silicon directly on the hemi-spherical grain silicon.

18. The method of claim 17, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

19. The method of claim 17, wherein the hemi-spherical grain silicon is formed by decomposing DCS ($Si_2H_2Cl_2$) in an H_2 and HCl environment at about 800 to 1000°C.

20. The method of claim 17, wherein the epitaxial silicon thickness is approximately 100Angstroms.

21. The method of claim 17, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

22. The method of claim 21, wherein the number of cycles performed is 5 cycles

23. The method of claim 17, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

24. A method of forming a capacitor structure for a semiconductor assembly during fabrication thereof comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material;

forming epitaxial silicon directly on the hemi-spherical grain silicon;

removing undesired regions of the hemi-spherical grain silicon and the epitaxial silicon to form a storage node capacitor plate;

forming a capacitor dielectric over the storage node capacitor plate; and

forming a capacitor top plate over the capacitor dielectric.

25. The method of claim 24, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

26. The method of claim 24, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

27. A semiconductor structure with a textured-surface for a semiconductor assembly comprising:

a hemi-spherical grain silicon on a supporting substrate; and

an epitaxial silicon directly on the hemi-spherical grain silicon.

28. The semiconductor structure of claim 27, further comprising an amorphous silicon layer underlying the hemi-spherical grain silicon.

29. The semiconductor structure of claim 27, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

30. The semiconductor structure of claim 27, wherein the epitaxial silicon thickness is approximately 100Angstroms.

31. The semiconductor structure of claim 27, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

32. A memory cell for a semiconductor assembly comprising:

an access transistor to a storage capacitor;

a conductive plug connecting to a source/drain of the access transistor;

a hemi-spherical grain silicon overlying the conductive plug; and

an epitaxial silicon directly on the hemi-spherical grain silicon.

33. The memory cell of claim 32, further comprising an amorphous silicon layer between the source/drain region of the access transistor and the conductive plug.

34. The memory cell of claim 32, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

35. A capacitor plate for a semiconductor assembly comprising:

a hemi-spherical grain silicon connecting to a conductive material; and

an epitaxial silicon directly on the hemi-spherical grain silicon.

36. The capacitor plate of claim 35, wherein the conductive material comprises an underlying conductive polysilicon plug.

37. The capacitor plate of claim 35, wherein the conductive material comprises an amorphous silicon layer directly connecting to an underlying conductive polysilicon plug.

38. The capacitor plate of claim 35, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

39. The capacitor plate of claim 35, wherein the epitaxial silicon thickness is approximately 100Angstroms.

40. The capacitor of claim 35, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

41. A semiconductor assembly having a capacitor structure comprising;

an isolation material having a hole therein;

a hemi-spherical grain silicon residing in the hole and connecting to a conductive material;

an epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in the vertical direction that graduates down to less thickness in the horizontal direction;

a capacitor dielectric overlying the epitaxial silicon; and

a capacitor plate overlying the capacitor dielectric.

42. The semiconductor assembly of claim 41, wherein the conductive material comprises an underlying conductive polysilicon plug.

43. The semiconductor assembly of claim 41, wherein the conductive material comprises an amorphous silicon layer directly connecting to an underlying conductive polysilicon plug.